ABSTRACT OF THE DISCLOSURE

A controller arrangement for effectuating data transfer across a clock boundary between a core clock domain and a bus clock domain, wherein the core clock domain is operable with a core clock signal and the bus clock domain is operable with a bus clock signal. A bus clock synchronizer controller portion is operable to generate a set of clock relationship control signals, at least a portion of which signals are used in generating a set of bus domain synchronizer control signals towards bus-to-core and core-to-bus synchronizers. A core clock synchronizer controller portion is provided for generating a set of core domain synchronizer control signals towards the synchronizers. The core clock synchronizer controller portion is operable responsive to the clock relationship control signals as well as configuration information signals indicative of different skew tolerances and latency values associated with the clock signals.